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1. A method for displaying a number of selected cells on a cathode ray tube, wherein the number of selected cells are represented in a circuit design database, the method comprising the steps of:

a. generating a selection list of the selected cells;

b. selecting at least one of the selected cells; and

c. establishing a view frame around the at least one of the selected cells selected in step (b) by depressing a number of predefined hot keys.

2. A method according to claim 1 further comprising the step of receiving a number of user defined display options, wherein the user defined display options determine the display of the circuit design database in the established view frame.

3. A method according to claim 1 wherein said establishing step sequentially establishes a view frame around selected cells in the selection list when the number of hot key(s) are sequentially depressed.

4. A method according to claim 1 further comprising the step of selectively editing the circuit design database after the view frame is established.

5. A method according to 4 wherein the circuit design

database includes a number of levels of hierarchy, and wherein each of the selected cells has a predefined top level of hierarchy that corresponds to one of the number of levels of hierarchy in the circuit design database.

6. A method according to claim 5 wherein said establishing step includes the step of setting the hierarchical level, within a circuit design database editor, to a predetermined level that is at or above the predefined top level of hierarchy of the corresponding cell(s) when said establishing step establishes a view frame therearound.

7. A method according to claim 6 wherein said circuit design database is a physical design database representing a physical design of the circuit design.

8. A method according to claim 7 wherein said physical design database is a placement design database, representing a placement of predefined cells of the circuit design database.

9. A method according to claim 1 wherein said circuit design database is a schematic design database representing a schematic representation of the circuit design.

10. A method according to claim 1 wherein said circuit

design database is a simulation design database.

11. A method according to claim 1 wherein said generating step includes a physical violation checking step for identifying a number of physical violations in the circuit design database, and for identifying selected ones of the number of cells that caused selected ones of the number of physical violations.

12. A method according to claim 11 wherein said physical violations checking step checks for cell overlaps.

13. A method according to claim 11 wherein said physical violations checking step checks for parking lot violations.

14. A method according to claim 11 wherein said physical violations checking step checks for off-grid errors.

15. A method according to claim 11 wherein said physical violations checking step checks for out-of-context cells.

16. A method according to claim 11 wherein said generating step includes a timing violation checking step for identifying a number of timing violations in the circuit design, and for identifying selected ones of the number of cells that should be substituted with logically equivalent cells having a different drive strength to minimize the number of timing violations.

17. A method for sequentially viewing a number of selected cells, wherein the number of selected cells are represented in a circuit design database, the method comprising the steps of:

a. generating a selection list of the selected cells, wherein the selected cells are sequentially ordered in the selection list;

b. establishing a view frame around a first cell selected from the selection list when a predefined combination of hot keys are depressed; and

c. establishing a view frame around a next cell wherein the next cell sequentially follows the first cell in the selection list when the predefined combination of hot keys is again depressed.

18. A method according to claim 17 wherein step (c) is repeated until the remaining cells in the selection list have each had a view frame established therearound.

19. A method according to claim 17 further comprising the step of selectively editing the circuit design database after the view frame has been established around the first cell.

20. A method according to claim 19 further comprising the step of selectively editing the circuit design database after the view frame has been established around the next cell.

21. A method according to claim 19 wherein the circuit design database includes a number of levels of hierarchy, and wherein each of the number of selected cells has a predefined top level of hierarchy that corresponds to one of the number of levels of hierarchy in the circuit design database.

22. A method according to claim 21 further comprising the step of setting the hierarchical level to a predetermined level that is at or above the predefined top level of hierarchy of the first cell when said view frame is established therearound.

23. A method for sequentially viewing a number of selected cells, wherein the number of selected cells are represented in a circuit design database, the method comprising the steps of:

a. generating a selection list of the selected cells, wherein the selected cells are sequentially ordered in the selection list;

b. selecting a first cell from the selection list;

c. establishing a view frame around the first cell when a predefined combination of hot keys are depressed; and

d. establishing a view frame around a next cells wherein the next cell sequentially follows the first cell in the selection list when the predefined combination of hot keys is again depressed.

24. In a data processing system for designing a circuit design, wherein the circuit design is represented in a circuit design database including a number of cells, the improvement comprising:

a. cell selection list generating means for generating a list of selected ones of the number of cells included in the circuit design database;

b. viewing means coupled to said cell selection list generating means for establishing a view frame around at least one of the selected cells; and

c. user control means coupled to said viewing means for allowing a user to control around which of the selected cells that the view frame is established.

25. A data processing system according to claim 24 wherein said viewing means views the circuit design database according to a number of user defined display options.

26. A data processing system according to claim 24 wherein said user control means includes a hot key means, wherein the hot key means establishes the view frame around selected ones of the selected cells each time the hot key means is activated.

27. A data processing system according to claim 26 wherein said hot key mean is activated by depressing a number of predefined hot key(s).

28. A data processing system according to claim 24 further comprising a circuit design database editor for editing the circuit design database.

29. A data processing system according to 28 wherein the circuit design database includes a number of levels of hierarchy, and wherein each of the selected cells has a predefined top level of hierarchy that corresponds to one of the number of levels of hierarchy in the circuit design database.

30. A data processing system according to claim 29 wherein said circuit design database editor allows a user to modify the placement of a selected cell within the circuit design database when the level of hierarchy is set, within the circuit design database editor, to at or above the predefined top level of hierarchy for the selected cell.

31. A data processing system according to claim 30 further comprising a hierarchy control means coupled to said viewing means for setting the hierarchical level, within the circuit design database editor, to a predetermined level

that is at or above the predefined top level of hierarchy of the corresponding cell when said viewing means establishes a view frame therearound.

32. A data processing system according to claim 31 wherein said circuit design database is a physical design database representing a physical design of the circuit design.

33. A data processing system according to claim 32 wherein said physical design database is a placement design database, representing a placement of predefined cells of the circuit design database.

34. A data processing system according to claim 24 wherein said circuit design database is a schematic design database representing a schematic representation of the circuit design.

35. A data processing system according to claim 24 wherein said circuit design database is a simulation design database.

36. A data processing system according to claim 24 wherein said cell selection list generating means includes a physical violation checking means for identifying a number

of physical violations in the circuit design database, and for identifying selected ones of the number of cells that caused selected ones of the number of physical violations.

37. A data processing system according to claim 36 wherein said physical violations checking means checks for cell overlaps.

38. A data processing system according to claim 36 wherein said physical violations checking means checks for parking lot violations.

39. A data processing system according to claim 36 wherein said physical violations checking means checks for off-grid errors.

40. A data processing system according to claim 36 wherein said physical violations checking means checks for out-of-context cells.

41. A data processing system according to claim 36 wherein said cell selection list generating means includes a timing violation checking means for identifying a number of timing violations in the circuit design, and for identifying selected ones of the number of cells that should be substituted with logically equivalent cells having a

different drive strength to minimize the number of timing violations.